AK4709

Low Power AV SCART Switch

GENERAL DESCRIPTION

The AK4709 is an I^2C controlled audio and video switch which has a matrix designed architecture for digital TV and set-top-box applications. The AK4709 offers the ideal features for digital set-top-box systems. The AK4709 includes audio switches, video switches, and video filters. The integrated audio driver supports ground referenced outputs, eliminating the need for large AC-coupling capacitors, reducing cost and saving board space. The AK4709 is housed in a space saving small 48-pin LQFP package.

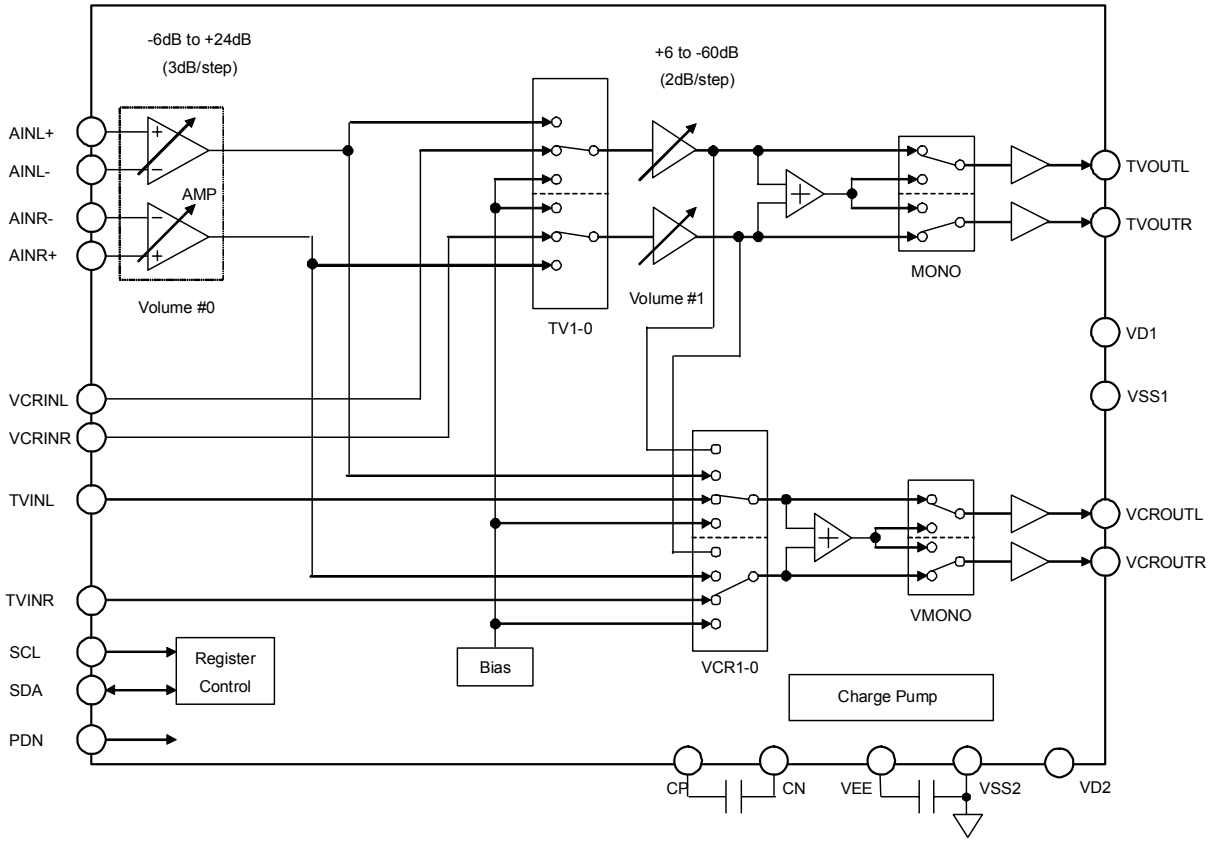
FEATURES

Analog switches for SCART
- **Audio section**
  - ☐ **THD+N: –95dB (@2Vrms)**
  - ☐ **Dynamic Range: 99dB (@2Vrms), (A-weighted)**
  - ☐ **Stereo Analog Volume with Pop-noise Free Circuit (+6dB to –60dB & Mute)**
  - ☐ **Analog Inputs**
    One Full Differential Stereo Input or Single-ended input for Decoder DAC
    Two Stereo Input (TV & VCR SCART)
  - ☐ **Analog Outputs**
    Two Stereo Outputs (TV & VCR SCART)
  - ☐ **Ground-Referenced Outputs Eliminate DC-Blocking Capacitor**
- **Video section**
  - ☐ **Integrated LPF: –40dB@27MHz**
  - ☐ **75ohm driver**
  - ☐ **6dB Gain for Outputs**
  - ☐ **Four CVBS/Y inputs (ENCx2, TV, VCR), Two CVBS/Y outputs (TV, VCR)**
  - ☐ **Three R/C inputs (ENCx2, VCR), Two R/C output (TV, VCR)**
  - ☐ **Two G and B inputs (ENC, VCR), One G and B outputs (TV)**
  - ☐ **Bi-Directional Control for VCR-Red/Chroma**
  - ☐ **Y/Pb/Pr Option (to 6MHz)**
- **TV/VCR input monitor**
- **Loop-through Mode for standby**
- **Auto-Startup Mode for power saving**
- **SCART pin#16 (Fast Blanking), pin#8 (Slow Blanking) Control**

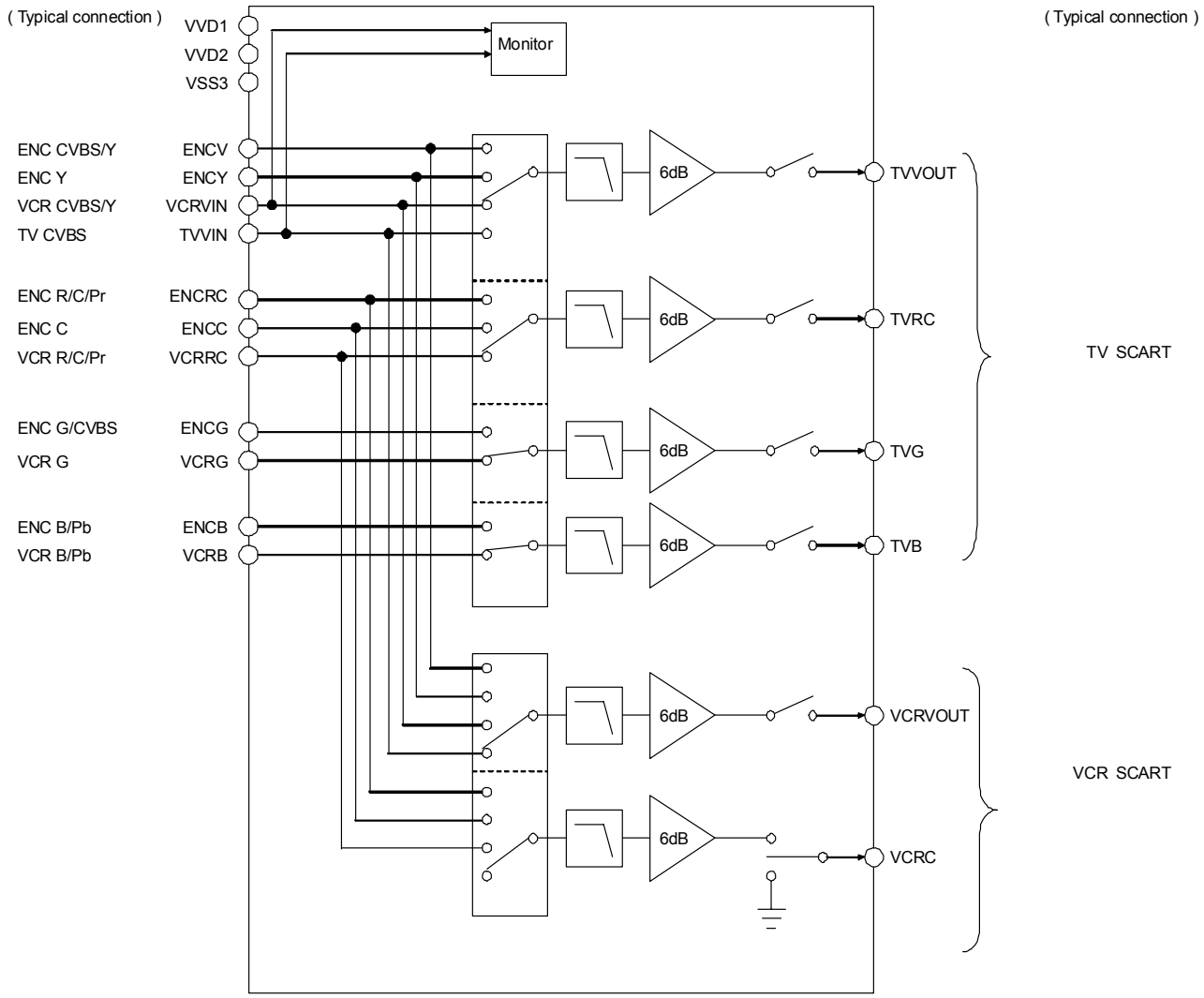
Power supply
- ☐ **3.3V+/–5% and 12V+/–10%**
- ☐ **Low Power Dissipation / Low Power Standby Mode**

Package
- ☐ **Small 48pin LQFP**

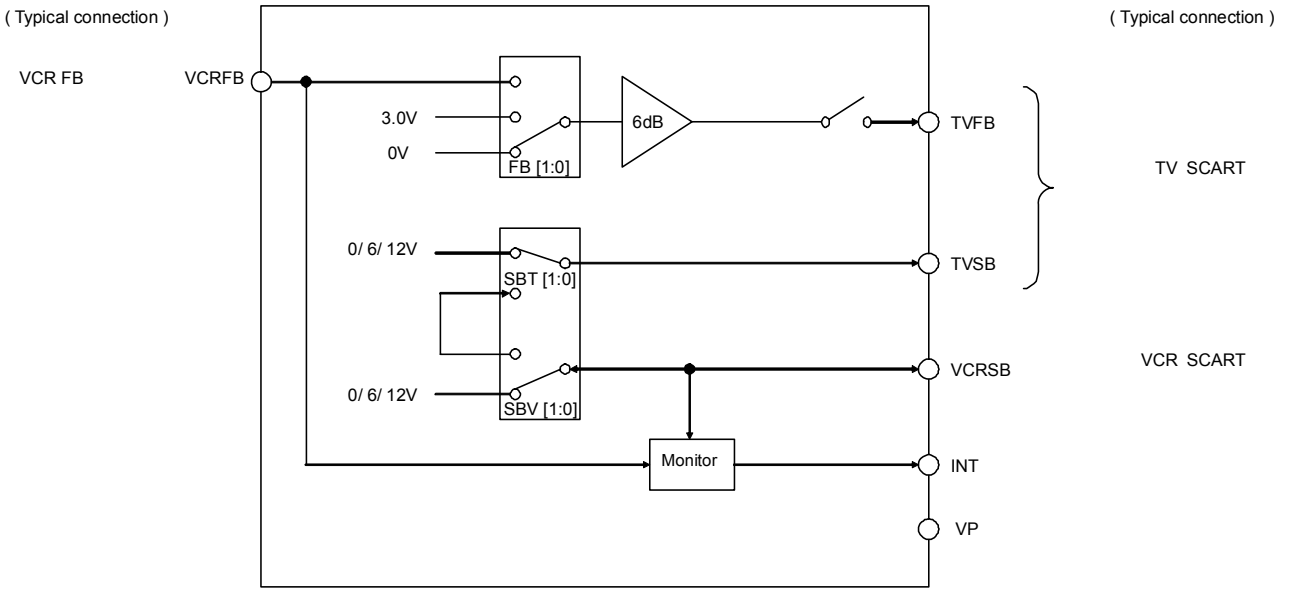
■ Block Diagram



Audio Block


(Typical connection)
VVD1
VVD2
VSS3
Monitor
ENC CVBS/Y
ENC Y
VCR CVBS/Y
TV CVBS
ENCV
ENCY
VCRVIN
TVVIN
ENC R/C/Pr
ENC C
VCR R/C/Pr
ENCRC
ENCC
VCRRC
ENC G/CVBS
VCR G
ENCG
VCRG
ENC B/Pb
VCR B/Pb
ENCB
VCRB
6dB
TVVOUT
TVRC
TVG
TVB
TV SCART
VCRVOUT
VCRC
VCR SCART
(Typical connection)

Video Block

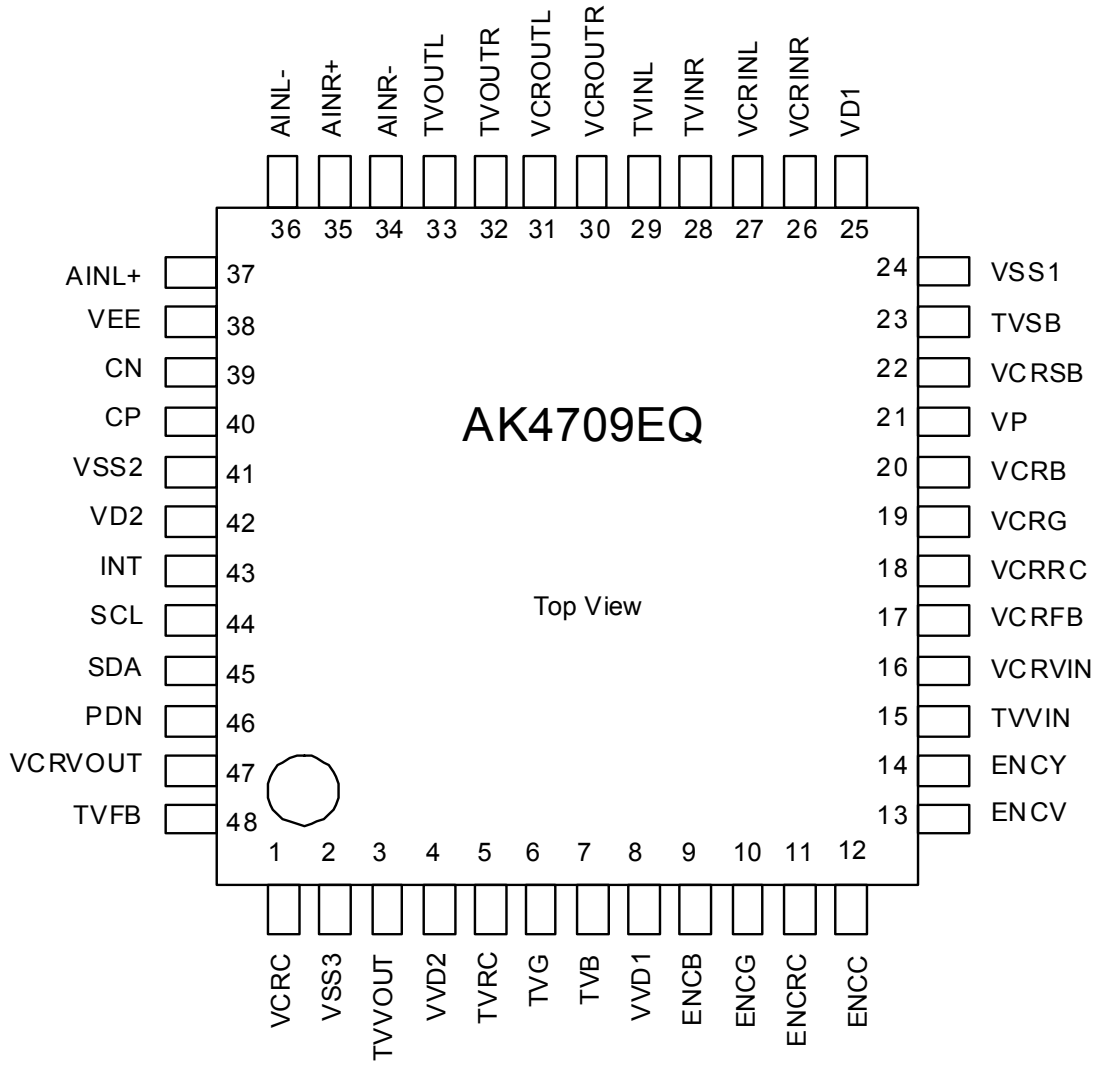


Video Blanking Block

■ Ordering Guide

AK4709EQ	-10 ~ +70°C	48pin LQFP (0.5mm pitch)
AKD4709	Evaluation board for AK4709	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VCRC	O	Chrominance Output Pin for VCR
2	VSS3	-	Video Ground Pin , 0V
3	TVVOUT	O	Composite/Luminance Output Pin for TV
4	VVD2	-	Video Power Supply Pin #2: 3.13V ~ 3.47V Normally connected to VSS3 with a 0.1µF ceramic capacitor in parallel with a 4.7µF electrolytic capacitor.
5	TVRC	O	Red/Chrominance Output Pin for TV
6	TVG	O	Green Output Pin for TV
7	TVB	O	Blue Output Pin for TV
8	VVD1	-	Video Power Supply Pin #1: 3.13V ~ 3.47V Normally connected to VSS3 with a 0.1µF ceramic capacitor in parallel with a 4.7µF electrolytic capacitor.
9	ENCB	I	Blue Input Pin for Encoder
10	ENCG	I	Green Input Pin for Encoder
11	ENCRC	I	Red/Chrominance Input Pin #1 for Encoder
12	ENCC	I	Chrominance Input Pin #2 for Encoder
13	ENCV	I	Composite/Luminance Input Pin #1 for Encoder
14	ENCY	I	Composite/Luminance Input Pin #2 for Encoder
15	TVVIN	I	Composite/Luminance Input Pin for TV
16	VCRVIN	I	Composite/Luminance Input Pin for VCR
17	VCRFB	I	Fast Blanking Input Pin for VCR
18	VCRRC	I	Red/Chrominance Input Pin for VCR
19	VCRG	I	Green Input Pin for VCR
20	VCRB	I	Blue Input Pin for VCR
21	VP	-	Blanking Power Supply Pin, 10.8V ~ 13.2V The VP pin must be connected to the Analogue 12V power supply via a 10ohm resistor and with a 0.1µF ceramic capacitor in parallel with a 1µF electrolytic capacitor to VSS1, as shown in Figure 20.
22	VCRSB	I/O	Slow Blanking Input/Output Pin for VCR, refer to Table 20. A 470ohm ±5% resistor must be connected between the VCRSB pin and SCART connector.
23	TVSB	O	Slow Blanking Output Pin for TV A 470ohm ±5% resistor must be connected between the TVSB pin and SCART connector.
24	VSS1	-	Audio Ground Pin , 0V
25	VD1	-	Audio Power Supply Pin: 3.13V ~ 3.47V Normally connected to VSS1 with a 0.1µF ceramic capacitor in parallel with a 4.7µF electrolytic capacitor.
26	VCRINR	I	Rch VCR Audio Input Pin
27	VCRINL	I	Lch VCR Audio Input Pin
28	TVINR	I	Rch TV Audio Input Pin
29	TVINL	I	Lch TV Audio Input Pin
30	VCROUTR	O	Rch Analog Output Pin #1
31	VCROUTL	O	Lch Analog Output Pin #1
32	TVOUTR	O	Rch Analog Output Pin #2
33	TVOUTL	O	Lch Analog Output Pin #2

No.	Pin Name	I/O	Function
34	AINRN	I	Rch Negative Analog Input Pin
35	AINRP	I	Rch Positive Analog Input Pin
36	AINLN	I	Lch Negative Analog Input Pin
37	AINLP	I	Lch Positive Analog Input Pin
38	VEE	O	Negative Voltage Output Pin Connect to VSS2 with a 1.0μF capacitor that should have the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the VSS2 pin. Non polarity capacitors can also be used.
39	CN	I	Negative Charge Pump Capacitor Terminal Pin Connect to CP with a 1.0μF capacitor that should have the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CP pin. Non polarity capacitors can also be used.
40	CP	I	Positive Charge Pump Capacitor Terminal Pin Connect to CN with a 1.0μF capacitor that should have the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CP pin. Non polarity capacitors can also be used.
41	VSS2	-	Charge Pump Ground Pin , 0V
42	VD2	-	Charge Pump Power Supply Pin: 3.13V ~ 3.47V Normally connected to VSS2 with a 0.1μF ceramic capacitor in parallel with a 4.7μF electrolytic cap.
43	INT	O	Interrupt Pin for Video Blanking Normally connected to VVD1(3.3V) through 10kΩ resistor externally.
44	SCL	I	I^2C Control Data Clock Pin
45	SDA	I/O	I^2C Control Data Pin
46	PDN	I	Power-Down Mode Pin When at "L", the AK4709 is in the power-down mode and is held in reset. The AK4709 should always be reset upon power-up.
47	VCRVOUT	O	Composite/Luminance Output Pin for VCR
48	TVFB	O	Fast Blanking Output Pin for TV

Note: SCL, SDA, PDN pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS1 =VSS2 =VSS3 = 0V; Note 1)

Parameter	Symbol	Min	max	Units
Power Supply (Note 2)	VD1	–0.3	4.0	V
	VD2	-0.3	4.0	V
	VVD1	–0.3	4.0	V
	VVD2	–0.3	4.0	V
	VP	–0.3	14	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Digital Input Voltage(PDN pin)	VIND1	–0.3	VVD1+0.3	V
Digital Input Voltage(SCL, SDA pins)	VIND2	–0.3	4.0	V
Video Input Voltage	VINV	–0.3	VVD1+0.3	V
Audio Input Voltage (Note 3)	VINA	VEE-0.3	VD1+0.3	V
Ambient Operating Temperature	Ta	–10	70	°C
Storage Temperature	Tstg	–65	150	°C

Note 1. All voltages with respect to ground.

Note 2. VSS1, VSS2 and VSS3 must be connected to the same analog ground plane.

Note 3. VEE: VEE pin voltage.

The internal negative power supply generating circuit provides negative power supply(VEE). The PDN pin, AUTO bit, MUTE bit, STBY bit and AMP bit control operation mode as shown in Table 2 and Table 3.

Mode			VEE pin Voltage
0	Full Power-down		0V
1	Auto Startup mode (Power-on default)	No video input	0V
		Video input	-VD2+0.2V
2	Standby & mute		0V
3	Standby		-VD2+0.2V
4	Mute		0V
5	Normal operation	No video input	0V
		Video input	-VD2+0.2V

Table 1. VEE pin voltage

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1 =VSS2 =VSS3 = 0V; Note 1)

Parameter	Symbol	Min	typ	max	Units
Power Supply (Note 4)	VD1	3.13	3.3	3.47	V
	VD2	3.13	3.3	3.47	V
	VVD1	3.13	3.3	3.47	V
	VVD2	3.13	3.3	3.47	V
	VP	10.8	12	13.2	V

Note 1. All voltages with respect to ground.
Note 4. VVD1 and VVD2 must be connected to the same voltage.

*AKM assumes no responsibility for the usage beyond recommended operating conditions in this datasheet.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C; VP = 12V, VD1 = VD2 = VVD1 = VVD2 = 3.3V)

Power Supplies		min	typ	max	Units
Power Supply Current					
Normal Operation (PDN = "H")					
VD1+VD2+VVD1+VVD2	(No load, Note 5)		0.49	0.74	mA
VD1+VD2+VVD1+VVD2	(With load, Note 6)		85		mA
VP			80	120	μA
Power-Down Mode (PDN = "L")	(Note7)				
VD1+VD2			0	10	μA
VVD1+VVD2			0	10	μA
VP			80	120	μA

Note 5. STBY bit = "0", All video outputs active. No signal, no load for A/V switches.
Note 6. All video outputs active.
Audio Output: 1kHz 2Vrms output with 4.5kΩ load at all audio output pins.
Video Output: 100% color bar output with 150Ω load at all video output pins.
Slow Blanking (default setting): SBIO1-0 bits= "00", SBT1-0 bits= "00", SBV1-0 bits= "00"
Note7. All digital inputs are held at VVD1 or VSS3. No signal, no load for A/V switches.

DIGITAL CHARACTERISTICS

(Ta = 25°C; VD1 = VD2 = VVD1 = VVD2 = 3.13 ~ 3.47V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VVD1	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VVD1	V
Low-Level Output Voltage (SDA pin: Iout= 3mA, INT pin: Iout= 1mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	± 10	μA

ANALOG CHARACTERISTICS (AUDIO)

(Ta=25°C; VP=12V, VD1=VD2=VVD1=VVD2=3.3V; Signal Frequency=1kHz; Measurement frequency=20Hz ~ 20kHz; R_L ≥4.5kΩ; 0dB=2Vrms output; Volume#0=Volume#1=0dB, unless otherwise specified)

Parameter	min	typ	max	Units
Analog Input: (TVINL/TVINR/VCRINL/VCRINR pins)				
Analog Input Characteristics				
Input Voltage (Note 6)			2.0	Vrms
Input Resistance	100	150	-	kΩ
Analog Input: (AINL+/AINL-/AINR-/AINR+ pins)				
Analog Input Characteristics				
Input Voltage (AIN+) – (AIN–), (Note 6)			2.0	Vrms
Input Resistance	80	125		kΩ
Stereo/Mono Output: (TVOUTL/TVOUTR/VCROUTL/VCROUTR pins) (Note 7)				
Analog Output Characteristics				
Volume#0 Step Width	2.3	3.0	3.7	dB
Volume#1 Step Width (+6dB to –12dB) (-12dB to –40dB) (-40dB to –60dB)	1.6 0.5 0.1	2 2 2	2.4 3.5 3.9	dB dB dB
THD+N (at 2Vrms, Note 9, Note 10, Note 11)		–95	–84	dB
Dynamic Range (–60dB Output, A-weighted, Note 9)	92	99		dB
S/N (A-weighted) (2Vrms output , Vo1#0=Vo1#1=0dB, Note 9, Note 13)	92	99		dB
Interchannel Isolation (Note 9, Note 12)	80	110		dB
Interchannel Gain Mismatch (Note 9, Note 12)	-0.5	0	+0.5	dB
DC offset (Note 14)	-5	0	+5	mV
Gain Drift	-	200	-	ppm/°C
Load Resistance TVOUTL/R, VCROUTL/R	4.5			kΩ
Load Capacitance TVOUTL/R, VCROUTL/R			20	pF
Output Voltage (Note 8)	1.85	2	2.15	Vrms
Power Supply Rejection (PSR) (Note 15)	-	50		dB

Note 6. f = 1kHz, THD+N < -80dB, gain = 0dB(Volume#0=Volume#1=0dB)

Note 7. Measured by Audio Precision System Two Cascade.

Note 8. The output level of the internal AMP with volume #0 should be less than 2Vrms.
The output level must be adjusted by the volume #1 when output level of the AK4709 exceeds 2Vrms.
The audio output must not exceed 2.15Vrms.

Note 9. Analog In to TVOUT/VCROUT.
Path: AINL+/- → TVOUTL, AINR+/- → TVOUTR, AINL+/- → VCROUTL, AINR+/- → VCROUTR
Volume#0=Volume#1=0dB.

Note 10. Differential Input. -86dB(typ) at VD= 3.13V
When single-ended Input,-90dB(typ) at f = 1kHz. -75dB(typ) at f = 10kHz

Note 11. -78dB (typ) referred to 0.5Vrms output level at Volume#0=+24dB, Volume#1= 0dB.
-80dB (typ) reffered to 0.5Vrms output level at Volume#0 = +21dB, Volume#1=0dB
Path: AINL+/- → TVOUTL, AINR+/- → TVOUTR, AINL+/- → VCROUTL, AINR+/- → VCROUTR

Note 12. Between TVOUTL and TVOUTR with analog inputs AINL+/–, AINL/R+/–, 1kHz/0dB.

Note 13. Analog In to TVOUT/VCROUT.
Path: AINL+/- → TVOUTL, AINR+/- → TVOUTR, AINL+/- → VCROUTL, AINR+/- → VCROUTR
81dB (typ) volume#0 = +24dB, Volume#1= 0dB
83dB (typ) volume#0 = +21dB, Volume#1= 0dB

Note 14. Analog In to TVOUT. Volume#0=Volume#1=0dB
Path: AINL+/- → TVOUTL, AINR+/- → TVOUTR, VCRINL → TVOUTL, VCRINR → TVOUTR

Note 15. The PSR is applied to VD1 and VD2 with 1kHz, 100mV.

ANALOG CHARACTERISTICS (VIDEO)

(Ta = 25°C; VP = 12V, VD1=VD2= VVD1 = VVD2 = 3.3V; unless otherwise specified.)

Parameter	Conditions	min	typ	max	Units
Sync Tip Clamp Voltage	at output pin.		0.24		V
R/G/B Clamp Voltage	at output pin.		0.24		V
Pb/Pr Clamp Voltage	at output pin.		1.49		V
Chrominance Bias Voltage	at output pin.		1.49		V
Gain	Input = 0.3Vp-p, 100kHz	5.5	6	6.5	dB
Interchannel Gain Mismatch1	TVRC, TVG, TVB. Input = 0.3Vp-p, 100kHz.	-0.5	-	0.5	dB
Interchannel Gain Mismatch2	VCRC, VCRGO, VCRBO. Input = 0.3Vp-p, 100kHz.	-0.5	-	0.5	dB
Frequency Response	Input=0.3Vp-p, C1=C2=0pF. 100kHz to 6MHz. at 10MHz. at 27MHz.	-1.0	 -3 -40	0.5 -20	dB dB dB
Group Delay Distortion	At 4.43MHz with respect to 1MHz.			20	ns
Input Impedance	Chrominance input (internally biased)	40	60	-	kΩ
Input Signal	f = 100kHz, maximum with distortion < 1.0%, gain = 6dB.	-	-	1.25	Vpp
Load Resistance	(Figure 1)	150	-	-	Ω
Load Capacitance	C1 (Figure 1) C2 (Figure 1)			400 15	pF pF
Dynamic Output Signal	f = 100kHz, maximum with distortion < 1.0%	-	-	2.5	Vpp
Y/C Crosstalk	f = 4.43MHz, 1Vp-p input. Among TVVOUT, TVRC and VCRVOUT outputs.	-	–50	-	dB
S/N	Reference Level = 0.7Vp-p, CCIR 567 weighting. BW = 15kHz to 5MHz.	-	74	-	dB
Differential Gain	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.	-	0.6	-	%
Differential Phase	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.	-	0.8	-	Degree

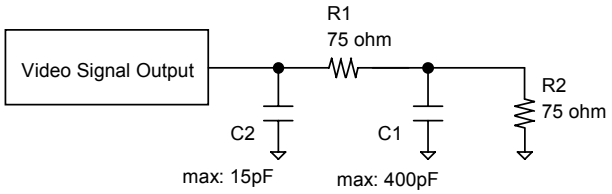


Figure 1. Load Resistance R1+R2 and Load Capacitance C1/C2.

SWITCHING CHARACTERISTICS

(Ta = 25°C; VP = 10.8 ~ 13.2V, VD1=VD2= VVD1 = VVD2 = 3.13 ~ 3.47V)

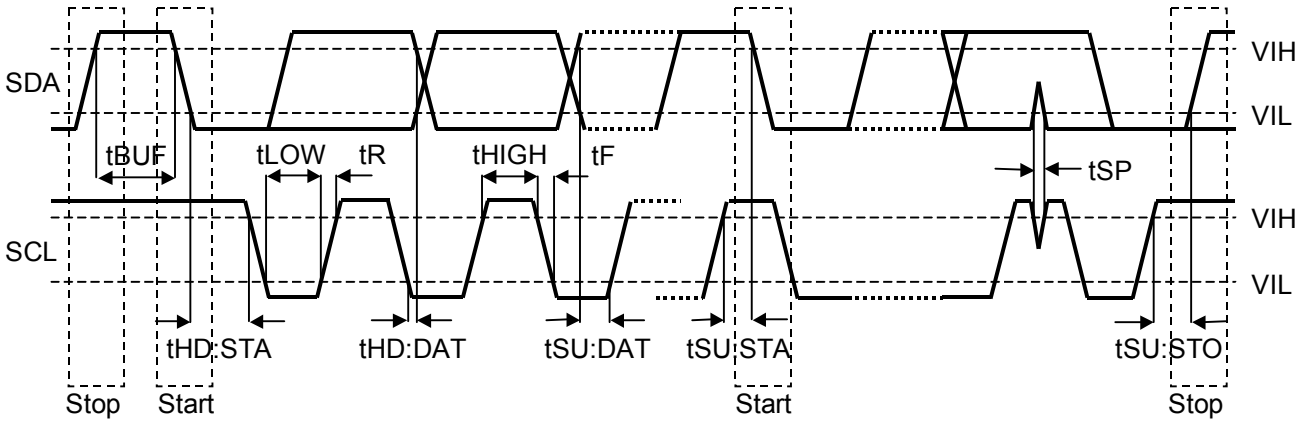
Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 16)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF
Reset Timing					
PDN Pulse Width (Note 17)	tPD	150			ns

Note 16. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

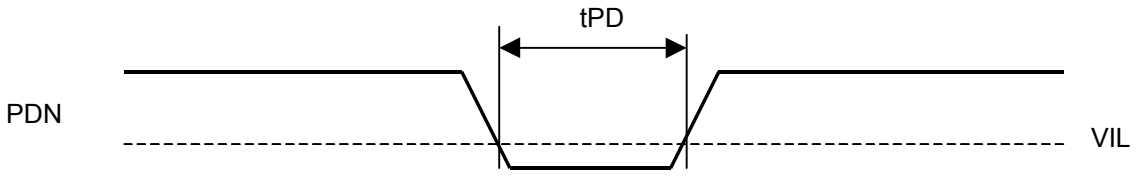
Note 17. The AK4709 should be reset once by bringing the PDN pin = “L” after all power supplies are supplied.

Note 18. I^2C-bus is a trademark of NXP B.V.

■ **Timing Diagram**



I^2C Bus mode Timing



Power-down Timing

OPERATION OVERVIEW

1. System Reset and Power-down options

The AK4709 should be reset once by bringing PDN pin = "L" after all power supplies are supplied. The AK4709 has several operation modes. The PDN pin, AUTO bit, MUTE bit, STBY bit and AMP bit control operation mode as shown in Table 2and Table 3.

■ System Reset and Full Power-down Mode

The AK4709 should be reset once by bringing PDN pin = "L" after all power supplies are supplied.

PDN pin: Power down pin
- L: Full Power-down Mode. Power-down, reset and initializes the control register.
- H: Device active.

■ Auto Startup Mode

After the PDN pin is set to "H", the AK4709 is in the auto startup mode. In this mode, all blocks except for the video detection circuit are powered down (Low power mode). Once the video detection circuit detects video signal from TVVIN pin or VCRVIN pin, the AK4709 goes to the stand-by mode automatically and sends "L" pulse via INT pin. The sources of TVOUTL/R are fixed to VCRINL/R, the sources of VCROUTL/R are fixed to TVINL/R respectively. The source of DC- restore circuit is VCRVIN pin. To exit the auto startup mode, set the AUTO bit to "0".

AUTO bit (00H D3): Auto startup bit
- 0: Auto startup disable. (Manual startup)
- 1: Auto startup enable. (default)

■ Mute Mode

When the MUTE bit = "1" and AUTO bit= "0", the audio outputs settle to VSS(0V, typ) and the charge pump circuit is in power down mode.

MUTE bit (00H D1): Audio output control
- 0: Normal operation.
- 1: All audio outputs to GND (default)

■ Standby Mode

When the AUTO bit = MUTE bit = "0" and the STBY bit = "1", the AK4709 is forced into TV-VCR loop through mode. In this mode, the sources of TVOUTL/R pins are fixed to VCRINL/R pins; the sources of VCROUTL/R are fixed to TVINL/R pins respectively. All register values are NOT changed by STBY bit = "1".

STBY bit (00H D0): Standby bit
- 0: Normal operation.
- 1: Standby mode. (default)

Mode	PDN pin	AUTO bit	STBY bit	MUTE bit	Mode
0	"L"	x	x	x	Full Power-down
1	"H"	1	x	x	Auto Startup mode (Power-on default)
2	"H"	0	1	1	Standby & Mute
3	"H"	0	1	0	Standby
4	"H"	0	0	1	Mute (Note 19) (AMP power down)
5	"H"	0	0	0	Normal operation (AMP operation)

Note 19. TVOUTL/R are muted by Mute bit in the default state.

Table 2. Operation Mode Settings (x: Don't Care)

Mode			Register Control	Audio Charge pump	Video Output	TVFB	VCRSB TVSB	Power Consumption
0	Full Power-down		NOT available	Power down	Hi-Z	Hi-Z	Pull -down (Note 20)	1mW (typ)
1	Auto Startup mode (Power-on default)	No video input	Available	Power down	Hi-Z	Hi-Z	Pull -down (Note 20)	2.5mW(typ)
		Video input (Note 21)		Active	Active (Note 22)	Active	Active	290mW(typ) (Note 23)
2	Standby & mute			Power down	Hi-Z	Active	Active	2.5mW(typ) (Note 24)
					Active (Note 25)			260mW (typ) (Note 23)
3	Standby			Active	Hi-Z			2.5mW (typ) (Note 24)
					Active (Note 25)			290mW(typ) (Note 23)
4	Mute (AMP power down)			Power down	Hi-Z			2.5mW(typ) (Note 24)
					Active (Note 25)			260mW (typ) (Note 23)
5	Normal operation (AMP operation)	No video input		Power down	Hi-Z			2.5mW(typ)
		Video input		Active	Hi-Z			2.5mW(typ)
					Active (Note 25)			290mW(typ) (Note 23)

Note 20. Internally pulled down by 120kΩ (typ) resistor.
Note 21. Video input to TVVIN or VCRVIN.
Note 22. VCRC output 0V for termination.
Note 23. All video outputs active.
Audio Output: 1kHz 2Vrms output, Video Output: 100% color bar output.
Slow Blanking (default setting): SBIO1-0 bits= "00", SBT1-0 bits= "00", SBV1-0 bits= "00"
Note 24. All video Amp power down.
Note 25. The video output status is Hi-Z (default) when output enable register (05H) is "0", and it is Active when output enable register (05H) is "1".

Table 3. Status of each operation mode

■ Typical Operation Sequence (auto setup mode)

The Figure 2 shows an example of the system timing at auto startup mode.

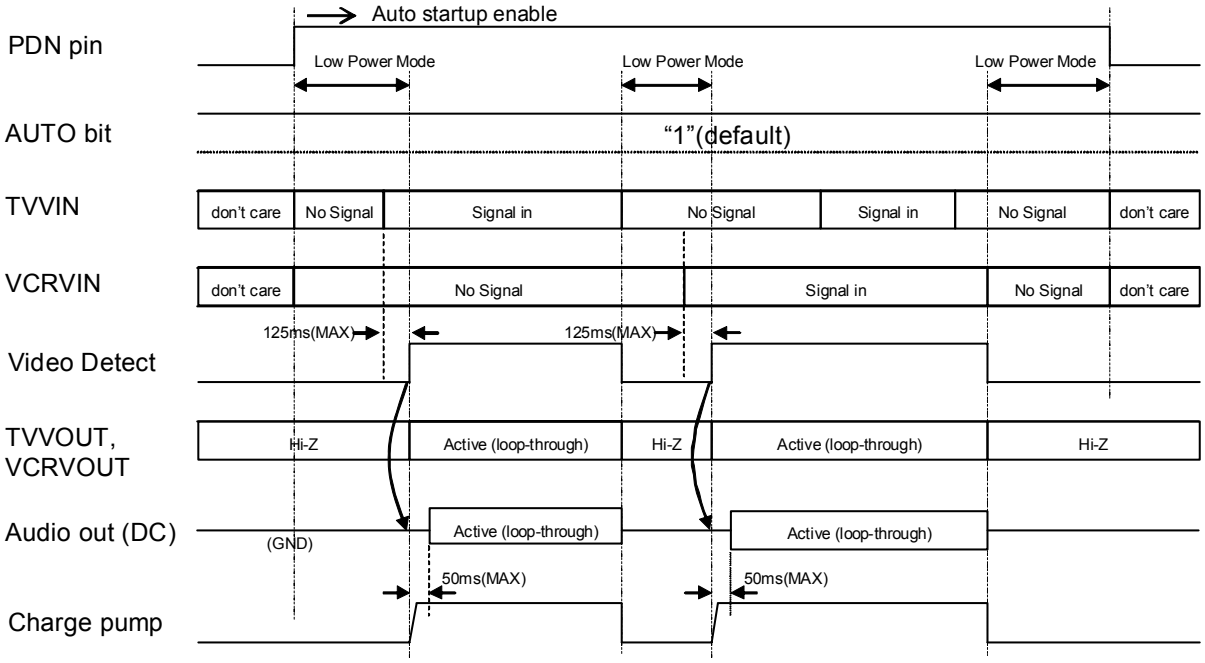
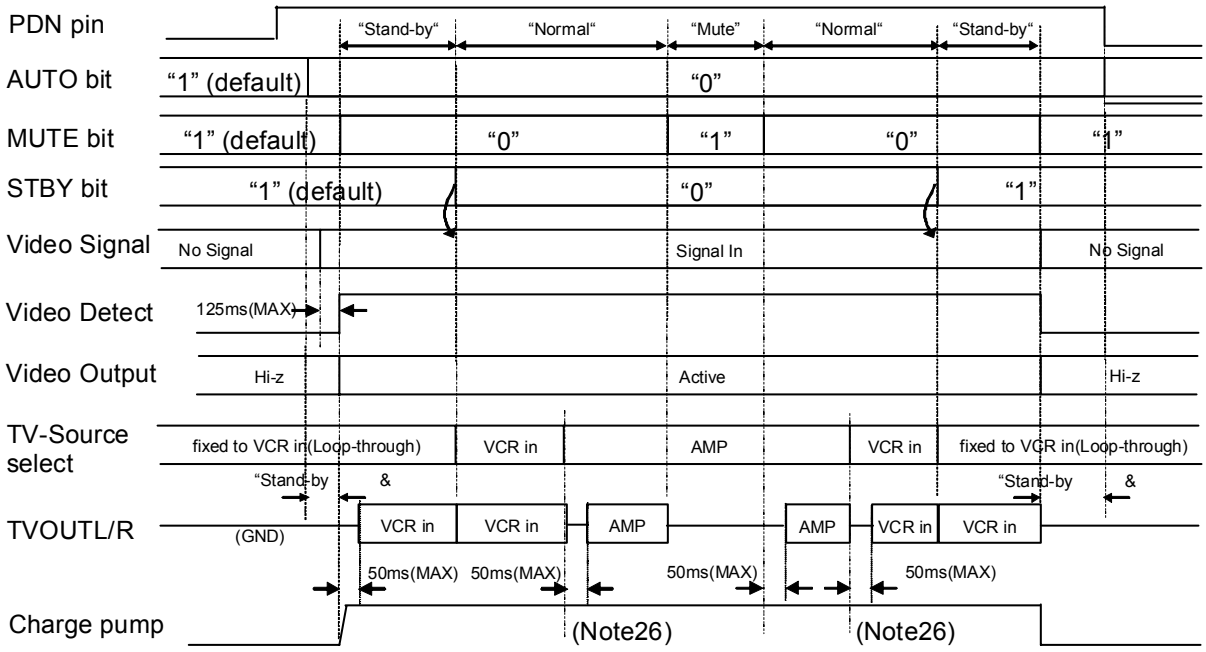


Figure 2. Auto Startup Mode Sequence

■ Typical Operation Sequence (except auto setup mode)

Figure 3 shows an example of the system timing at normal operation mode.



Note 26. Mute the analog outputs externally if click noise affects the system.

Figure 3. Typical Operating Sequence

2. Audio Block

■ Switch Control

The AK4709 has switch matrixes designed primarily for SCART routing. Those are controlled via the control register as shown in Table 4 and Table 5 (Please refer to the Block Diagram).

(01H: D1-D0)

TV1	TV0	Source of TVOUTL/R	
0	0	AMP	
0	1	VCRIN	(default)
1	0	Mute	
1	1	(Reserved)	

Table 4. TVOUT Switch Configuration

(01H: D5-D4)

VCR1	VCR0	Source of VCROUTL/R	
0	0	AMP	
0	1	TVIN	(default)
1	0	Mute	
1	1	Volume#1 output	

Table 5. VCROUT Switch Configuration

■ Volume Control #0 (11-Level Volume)

The AK4709 has a 11-level volume control (Volume #0) as shown in Table 6. The volume reflects the change of register value immediately.

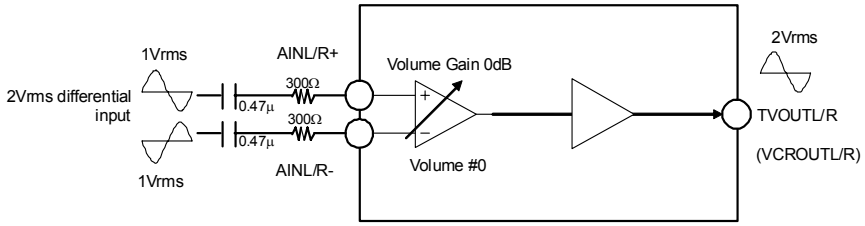


Figure 4. Volume #0(Volume Gain=0dB: default), Full Differential Stereo Input

(0DH: D6-D3)

VOL3	VOL2	VOL1	VOL0	Volume #0 Gain	Output Level (Typ)
1	1	x	x	NA	-
1	0	1	1	+24dB	2Vrms (with 0.13Vrms differential input)
1	0	1	0	+21dB	-
1	0	0	1	+18dB	2Vrms (with 0.25Vrms differential input)
1	0	0	0	+15dB	-
0	1	1	1	+12dB	2Vrms (with 0.5Vrms differential input)
0	1	1	0	+9dB	-
0	1	0	1	+6dB	2Vrms (with 1Vrms differential input)
0	1	0	0	+3dB	-
0	0	1	1	0dB	2Vrms (with 2Vrms differential input: default)
0	0	1	0	-3dB	-
0	0	0	1	-6dB	1Vrms (with 2Vrms differential input)
0	0	0	0	Mute	-

Note: Volume #1=0dB (x: Don't care)

Table 6. Volume #0, Full Differential Stereo Input

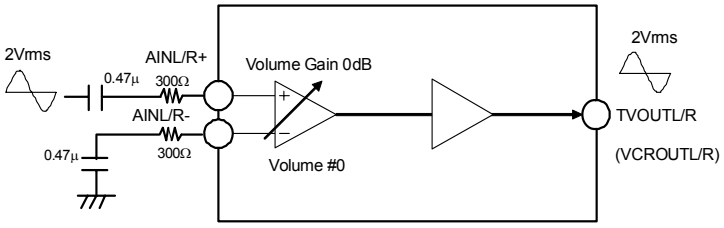


Figure 5. Volume #0(Volume Gain=0dB:default), Single-ended Input

(0DH: D6-D3)

VOL3	VOL2	VOL1	VOL0	Volume #0 Gain	Output Level (Typ)
1	1	x	x	NA	-
1	0	1	1	+24dB	2Vrms (with 0.13Vrms input)
1	0	1	0	+21dB	-
1	0	0	1	+18dB	2Vrms (with 0.25Vrms input)
1	0	0	0	+15dB	-
0	1	1	1	+12dB	2Vrms (with 0.5Vrms input)
0	1	1	0	+9dB	-
0	1	0	1	+6dB	2Vrms (with 1Vrms input)
0	1	0	0	+3dB	-
0	0	1	1	0dB	2Vrms (with 2Vrms input: default)
0	0	1	0	-3dB	-
0	0	0	1	-6dB	1Vrms (with 2Vrms input)
0	0	0	0	Mute	-

Note: Volume #1=0dB (x: Don't care)

Table 7. Volume #0, Single-ended Input

■ Volume Control #1 (Main Volume)

The AK4709 has main volume control (Volume #1) as shown in Table 8.

(02H: D5-D0)

L5	L4	L3	L2	L1	L0	Gain	
1	0	0	0	1	0	+6dB	
1	0	0	0	0	1	+4dB	
1	0	0	0	0	0	+2dB	
0	1	1	1	1	1	0dB	(default)
…	…	…	…	…	…	…	
0	0	0	0	0	1	-60dB	
0	0	0	0	0	0	Mute	

Note: The output must not exceed 2.15Vrms.

Table 8. Volume #1

When the MOD bit = "1"(default), changing volume levels does not cause pop noise. MDT1-0 bits select the transition time (Table 9). When the new gain value 1EH(-2dB) is written to gain resistor while the actual (stable) gain is 1FH(0dB), the gain changes to 1EH(-2dB) within the transition time selected by MDT1-0 bits. The built-in volume controller compares the actual gain to the value of gain register after finishing the transition time, and re-changes the actual gain to new resister value within the transition time if the register value is different from the actual gain when compared. When the MOD bit = "0" then there is no transition time and the gain changes immediately. This change may cause a click noise.

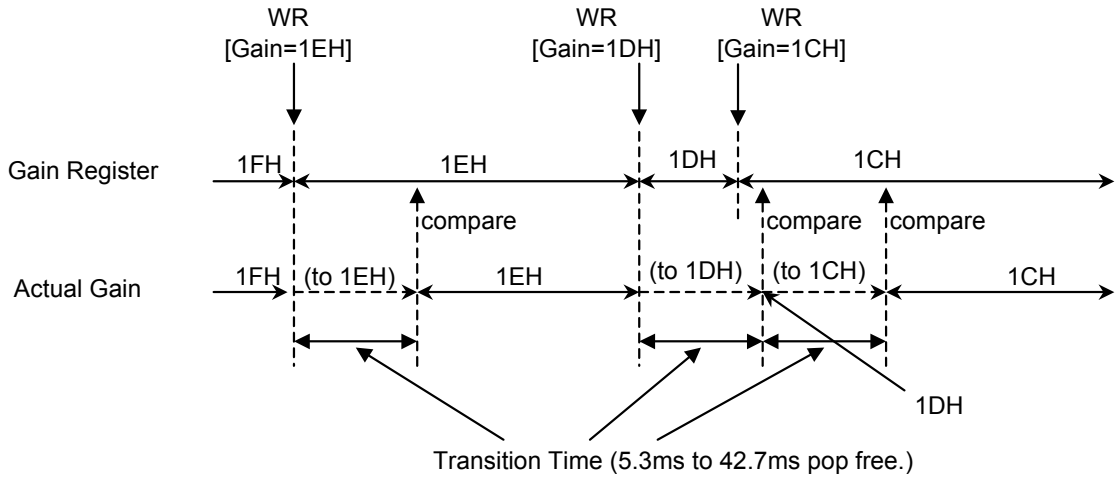


Figure 6. Volume Change Operation (MOD bit = "1")

MDT1	MDT0	Transition Time	
0	0	5.3ms	
0	1	10.7ms	
1	0	21.3ms	
1	1	42.7ms	(default)

Table 9. Volume Transition Time (typ.)

■ Analog output block

The AK4709 has chargepump circuit generating negative power supply rail from a 3.3V(typ) power supply. (Figure 7) It allows the AK4709 to output audio signal centered at VSS (0V, typ) as shown in Figure 8. Negative power generating circuit (Figure 7) needs 1.0uF capacitors (Ca, Cb) with low ESR (Equivalent Series Resistance). When using capacitors with a polarity, the positive side should be connected to CP and VSS2 for capacitor Ca and Cb, respectively. When the MUTE bit = "1", the charge pump circuit is in power down mode and its analog outputs become VSS (0V, typ).

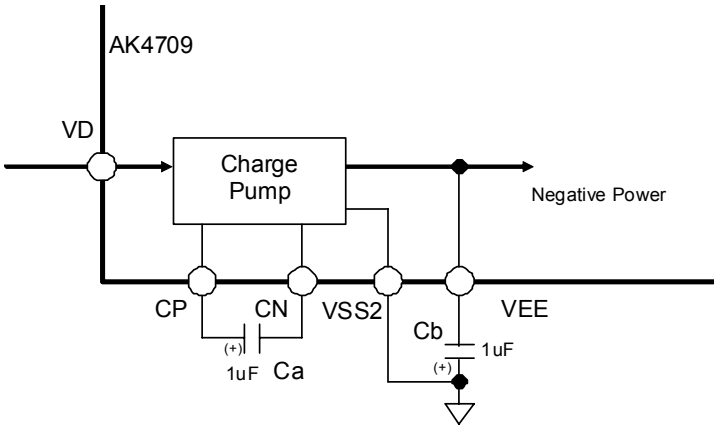


Figure 7. Negative power generate circuit

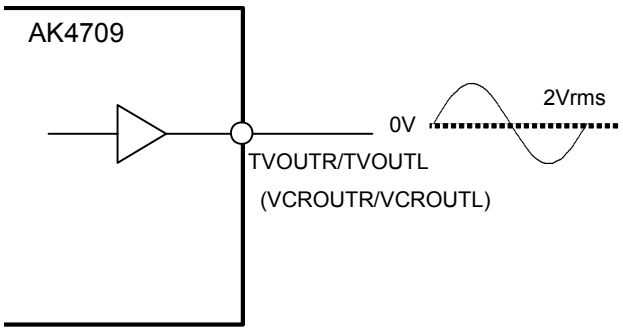


Figure 8. Audio signal output

3. Video Block

■ Video Switch Control

The AK4709 has switches for TV and VCR. Each switch can be controlled via the registers independently. When AUTO bit = "1" or STBY bit = "1", these switches setting is ignored and set to fixed configuration (loop-through mode). Please refer the auto startup mode and standby mode.

(04H: D2-D0)

Mode	VTV2-0 bit	Source of TVVOUT pin	Source of TVRC pin	Source of TVG pin	Source of TVB pin
Shutdown	000	(Hi-Z)	(Hi-Z)	(Hi-Z)	(Hi-Z)
Encoder CVBS+RGB or Encoder YPbPr	001	ENCV pin (Encoder CVBS or Y)	ENCRC pin (Encoder Red,C or Pb)	ENCG pin (Encoder Green or Y)	ENCB pin (Encoder Blue or Pr)
Encoder Y/C 1	010	ENCV pin (Encoder Y)	ENCRC pin (Encoder C)	(Hi-Z)	(Hi-Z)
Encoder Y/C 2	011	ENCY pin (Encoder Y)	ENCC pin (Encoder C)	(Hi-Z)	(Hi-Z)
VCR (default)	100	VCRVIN pin (VCR CVBS or Y)	VCRRC pin (VCR Red,C or Pb)	VCRG pin (VCR Green or Y)	VCRB pin (VCR Blue or Pr)
TV CVBS	101	TVVIN pin (TV CVBS)	(Hi-Z)	(Hi-Z)	(Hi-Z)
(Reserved)	110	-	-	-	-
(Reserved)	111	-	-	-	-

Table 10. TV video output (Note 27)

(04H: D5-D3)

Mode	VVCR2-0 bit	Source of VCRVOUT pin	Source of VCRC pin
Shutdown	000	(Hi-Z)	(Hi-Z)
Encoder CVBS or Y/C 1	001	ENCV pin (Encoder CVBS or Y)	ENCRC pin (Encoder C)
Encoder CVBS or Y/C 2	010	ENCY pin (Encoder CVBS or Y)	ENCC pin (Encoder C)
TV CVBS (default)	011	TVVIN pin (TV CVBS)	(Hi-Z)
VCR	100	VCRVIN pin (VCR CVBS)	VCRRC pin (VCR Red, C)
(Reserved)	101	-	-
(Reserved)	110	-	-
(Reserved)	111	-	-

Table 11. VCR video output (Refer Note 27)

Note 27. When input the video signal via ENCRC pin or VCRRC pin, set CLAMP1-0 bits respectively.

■ Video Output Control (05H: D6-D0,)

Each video output can be set to Hi-Z individually via the control registers. These settings are ignored when the AUTO bit = "1".

TVV: TVVOUT output control
TVR: TVRCOUT output control
TVG: TVGOUT output control
TVB: TVBOUT output control
VCRV: VCRVOUT output control
VCRC: VCRC output control
TVFB: TVFB output control
0: Hi-Z. (default)
1: Active.

■ RGB/Chroma Bi-directional Control for VCR SCART (05H: D7, D5)

The AK4709 supports the bi-directional RGB/Chroma signal on the VCR SCART.

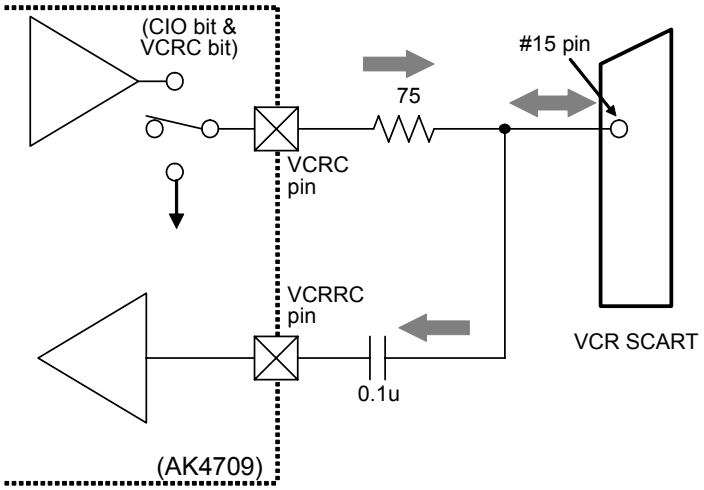


Figure 9. VCR Red/Chroma Bi-directional Control

CIO	VCRC	State of VCRC pin	
0	0	Hi-z	(default)
0	1	Active	
1	0	Connected to GND	
1	1	Connected to GND	

Table 12. VCR Red/Chroma Bi-directional Control

■ Clamp and DC-restore circuit control (06H: D7-D2)

Each CVBS and Y input has the sync tip clamp circuit. The DC-restore circuit has two clamp voltages 0.24V(typ) and 1.49V(typ) to support both RGB and YPbPr signal. They correspond to 0.12V(typ) and 0.75V(typ) at the SCART connector when matched by 75Ω resistors. The CLAMP1, CLAMP0 and CLAMPB bits select the input circuit for ENCRC pin (Encoder Red/Chroma), ENCB pin (Encoder Blue), VCRRC pin (VCR Red/Chroma) and VCRB pin (VCR Blue) respectively. VCLP2-0 bits select the sync source of DC- restore circuit.

CLAMPB	CLAMP0	VCRRC Input Circuit	VCRB Input Circuit	note	
0	0	DC restore clamp active (0.24V at sync timing/output pin)	DC restore clamp active (0.24V at sync timing/output pin)	for RGB	
0	1	Biased (1.49V at sync timing/output pin)	(DC restore clamp active) (0.24V at sync timing output pin)	for Y/C	(default)
1	0	DC restore clamp active (1.49V at sync timing/output pin)	DC restore clamp active (1.49V at sync timing/output pin)	for Y/Pb/Pr	
1	1	(reserved)	(reserved)		

Table 13. DC-restore control for VCR Input

CLAMPB	CLAMP1	ENCRC Input Circuit	ENCB Input Circuit	note	
0	0	DC restore clamp active (0.24V at sync timing/output pin)	DC restore clamp active (0.24V at sync timing/output pin)	for RGB	(default)
0	1	Biased (1.49V at sync timing/output pin)	DC restore clamp active (0.24V at sync timing output pin)	for Y/C	
1	0	DC restore clamp active (1.49V at sync timing/output pin)	DC restore clamp active (1.49V at sync timing/output pin)	for Y/Pb/Pr	
1	1	(reserved)	(reserved)		

Table 14. DC-restore control for Encoder Input

CLAMP2	ENCG Input Circuit	note	
0	DC restore clamp active (0.24V at sync timing/output pin)	for RGB	(default)
1	Sync tip clamp active (0.24V at sync timing/output pin)	for Y/Pb/Pr	

Note: When the VTV2-0 bits = “001” (source for TV = Encoder CVBS /RGB), TVG bit = “1” (TVG = active) and VCLP1-0 bits = “11” (DC restore source = ENCG), the sync tip is selected even if the CLAMP2 bit = “0”.

Table 15. DC-restore control for Encoder Green/Y Input

VCLP2-0: DC restore source control

VCLP2	VCLP1	VCLP0	Sync Source of DC Restore	
0	0	0	ENCV	(default)
0	0	1	ENCY	
0	1	0	VCRVIN	
0	1	1	ENCG	
1	0	0	VCRG	
1	0	1	(reserved)	
1	1	0	(reserved)	
1	1	1	(reserved)	

Note: When the AUTO bit = “1”, the source is fixed to VCRVIN.

Table 16. DC-restore source control

4. Blanking Control

The AK4709 supports Fast Blanking signals and Slow Blanking (Function Switching) signals for TV/VCR SCART.

■ Input/Output Control for Fast/Slow Blanking

FB1-0: TV Fast Blanking output control (07H: D1-D0)

FB1 bit	FB0 bit	TVFB pin Output Level	
0	0	0V	(default)
0	1	2V< 3.0V(typ) at 150Ω load	
1	0	Same as VCR FB input (2.5V/0V)	
1	1	(Reserved)	

Table 17. TV Fast Blanking output (Note: minimum load is 150Ω)

SBT1-0: TV Slow Blanking output control (07H: D3-D2)

SBT1 bit	SBT0 bit	TVSB pin Output Level	
0	0	< 2V	(default)
0	1	4.73V <, < 7V	
1	0	(Reserved)	
1	1	10V <	

Table 18. TV Slow Blanking output (Note: minimum load is 10kΩ)

SBV1-0: VCR Slow Blanking output control (07H: D5-D4)

SBV1 bit	SBV0 bit	VCRSB pin Output Level	
0	0	< 2V	(default)
0	1	4.73V <, < 7V	
1	0	(Reserved)	
1	1	10V <	

Table 19. VCR Slow Blanking output (Note: minimum load is 10kΩ)

SBIO1-0: TV/VCR Slow Blanking I/O control (07H: D7-D6)

SBIO1 bit	SBIO0 bit	VCRSB pin Direction	TVSB pin Direction	
0	0	Output (Controlled by SBV1-0 bits)	Output (Controlled by SBT1-0 bits)	(default)
0	1	(Reserved)	(Reserved)	
1	0	Input (Stored in SVCR1-0 bits)	Output (Controlled by SBT1-0 bits)	
1	1	Input (Stored in SVCR1-0 bits)	Output (Same output as VCR SB)	

Table 20. TV/VCR Slow Blanking I/O control

5. Monitor Options and INT function

■ Monitor Options (08H: D4-D0)

The AK4709 has several detection functions. SVCR1-0 bits, FVCR bit, VCMON bit and TVMON bit reflect the input DC level of VCR slow blanking, the input DC level of VCR fast blanking and signals input to TVVIN or VCRVIN pins.

SVCR1-0: VCR Slow blanking status monitor

SVCR1-0 bits reflect the voltage at VCRSB pin only when the VCRSB is in the input mode. When the VCRSB is in the output mode, SVCR1-0 bits hold previous value.

VCRSB pin input level	SVCR1 bit	SVCR0 bit
< 2V	0	0
4.5 to 7V	0	1
(Reserved)	1	0
9.5 <	1	1

Table 21. VCR Slow Blanking monitor

FVCR: VCR Fast blanking input level monitor

This bit is enabled when TVFB bit = "1".

VCRFB pin input level	FVCR bit
< 0.4V	0
1V <	1

Table 22. VCR Fast Blanking monitor (Typical threshold is 0.7V)

VCMON: VCRVIN pin video input monitor (MCOMN bit = "1"),
TVVIN pin or VCRVIN pin video input monitor (MCOMN bit = "0")

0: No video signal detected.
1: Detects video signal.

TVMON: TVVIN pin video input monitor (active when MCOMN bit = "1")

0: No video signal detected.
1: Detects video signal.

AUTO (00H D3)	MCOMN (09H D7)	TVVIN signal	VCRVIN signal	TVMON (08H D4)	VCMON (08H D3)
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	1
1	x	0	0	0	0
1	x	0	1	0	1
1	x	1	0	0	1
1	x	1	1	0	1

(x: don't care)

Note 28. TVVIN/VCRVIN signal: signal 0 = No signal applied, signal 1 = signal applied

Table 23. TV/VCR Monitor Function

■ INT Function and Mask Options (09H: D3-D1)

Changes of the 08H status can be monitored via the INT pin. The INT pin is an open drain output and goes "L" for 2μs (typ.) when the status of 08H is changed. This pin should be tied to VVD1 (typ. 3.3V) via 10kΩ resistor or lower voltage through 10kΩ resistor. MTV bit, MVC bit, MCOMN bit, MFVCR bit and MSVCR bit control the reflection of the status change of these monitors onto the INT pin from report to prevent to masks each monitor.

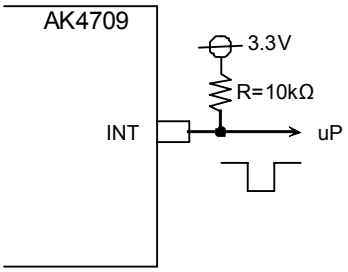


Figure 10. INT pin

MVC: VCMON Mask. Refer Table 25.
MTV: TVMON Mask. Refer Table 24.
MCOMN: Refer Table 23

AUTO (00H D3)	TVMON (08H D4)	MTV (09H D4)	INT
0	No Change	0	Hi-Z
0	No Change	1	Hi-Z
0	Change	0	Generates "L" Pulse
0	Change	1	Hi-Z
1	No Change	0	Hi-Z
1	No Change	1	Hi-Z

Note 29. When the STBY bit = "0", the TV Monitor Mask function is enabled.
Note 30. When AUTO bit = "1", TVMON does not change

Table 24. TV Monitor Mask

AUTO (00H D3)	VCMON (08H D3)	MVC (09H D3)	INT
0	No Change	0	Hi-Z
0	No Change	1	Hi-Z
0	Change	0	Generates "L" Pulse
0	Change	1	Hi-Z
1	No Change	0	Hi-Z
1	No Change	1	Hi-Z
1	Change	0	Generates "L" Pulse
1	Change	1	Generates "L" Pulse

Note 31. When the STBY bit = "0", the VCR Monitor Mask function is enabled.

Table 25. VCR Monitor Mask

MFVCR: FVCR Monitor mask.
0: Change of FVCR is reflected to INT pin. (default)
1: Change of FVCR is NOT reflected to INT pin.

MSVCR: SVCR1-0 Monitor mask
0: Change of SVCR1-0 is reflected to INT pin. (default)
1: Change of SVCR1-0 is NOT reflected to INT pin.

6. Control Interface (I^2C-bus Control)

1. WRITE Operations

Figure 11 shows the data transfer sequence in I^2C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 17). After the START condition, a slave address is sent. This address is 7bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010001". If the slave address match that of the AK4709, the AK4709 generates the acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 19). A "1" for R/W bit indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed. The second byte consists of the address for control registers of the AK4709. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 13). The data after the second byte contain control data. The format is MSB first, 8bits (Figure 14). The AK4709 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 17).
The AK4709 can execute multiple one byte write operations in a sequence. After receipt of the third byte, the AK4709 generates an acknowledge, and awaits the next data again. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 0DH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 19) except for the START and the STOP condition.

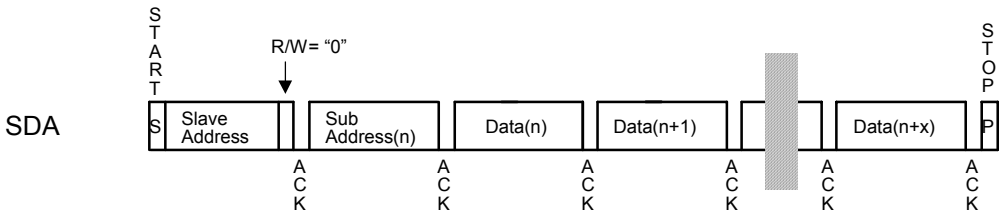


Figure 11. Data transfer sequence at the I^2C-bus mode

0	0	1	0	0	0	1	R/W

Figure 12. The first byte

0	0	0	A4	A3	A2	A1	A0

Figure 13. The second byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 14. Byte structure after the second byte

2. READ Operations

Set R/W bit = "1" for READ operations. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt the first data word. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 09H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4709 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

2-1. CURRENT ADDRESS READ

The AK4709 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to "1", the AK4709 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4709 discontinues transmission.

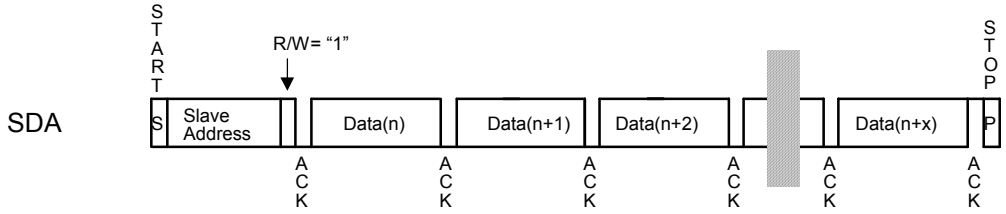


Figure 15. CURRENT ADDRESS READ

2-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start condition, slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4709 generates an acknowledge, 1-byte data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4709 discontinues transmission.

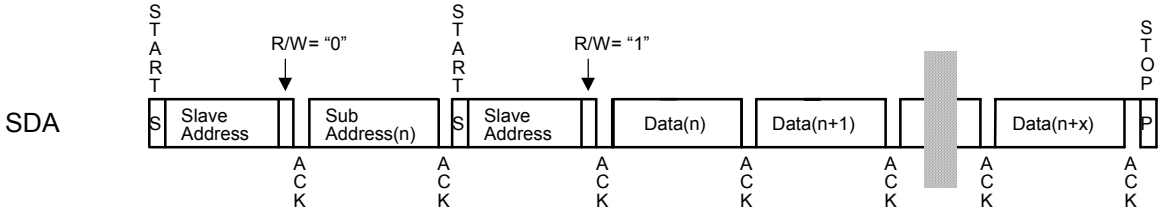


Figure 16. RANDOM ADDRESS READ

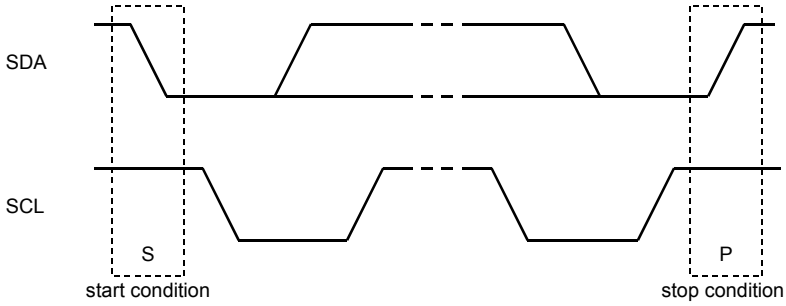


Figure 17. START and STOP conditions

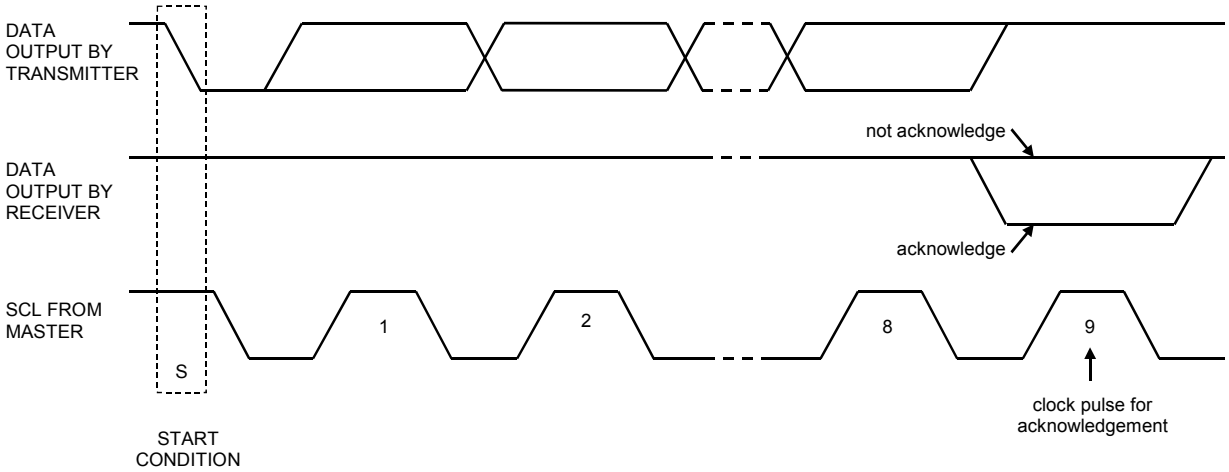


Figure 18. Acknowledge on the I^2C-bus

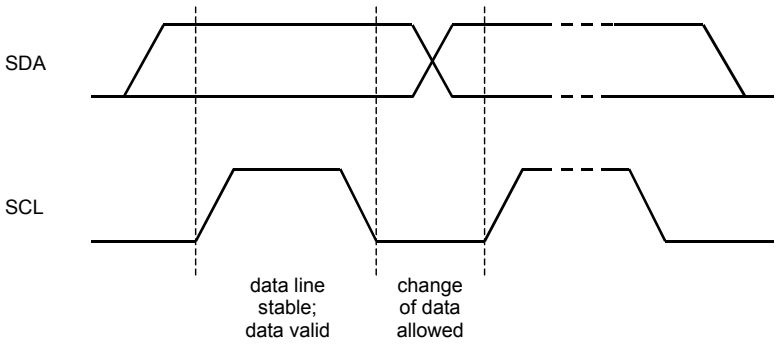


Figure 19. Bit transfer on the I^2C-bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	0	0	0	0	AUTO	0	MUTE	STBY
01H	Switch	VMUTE	0	VCR1	VCR0	MONO	1	TV1	TV0
02H	Main Volume	0	0	L5	L4	L3	L2	L1	L0
03H	Zerocross	0	VMONO	CAL	0	0	MOD	MDT1	MDT0
04H	Video switch	0	0	VVCR2	VVCR1	VVCR0	VTV2	VTV1	VTV0
05H	Video output enable	CIO	TVFB	VCRC	VCRV	TVB	TVG	TVR	TVV
06H	Video volume/clamp	CLAMPB	VCLP1	VCLP0	CLAMP2	CLAMP1	CLAMP0	0	0
07H	S/F Blanking control	SBIO1	SBIO0	SBV1	SBV0	SBT1	SBT0	FB1	FB0
08H	S/F Blanking monitor	0	0	FVCR1	TVMON	VCMON	FVCR0	SVCR1	SVCR0
09H	Monitor mask	MCOMN	0	0	MTV	MVC	MFVCR	MSVCR	0
0AH	DC restore	0	0	0	0	VCLP2	0	1	1
0BH	Reserved	0	0	0	0	0	0	0	0
0CH	Reserved	0	0	0	0	0	0	0	0
0DH	Volume	0	VOL3	VOL2	VOL1	VOL0	1	1	1

When the PDN pin goes “L”, the registers are initialized to their default values.
While the PDN pin = “H”, all registers can be accessed.
Do not write any data to the register over 0DH.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	0	0	0	0	AUTO	0	MUTE	STBY
R/W		R/W							
Default		0	0	0	0	1	0	1	1

STBY: Standby control
0: Normal Operation
1: Standby Mode (default). All registers are not initialized.
AMP: Powered down and timings are reset.
Source of TVOUT: fixed to VCRIN.
Source of VCROUT: fixed to TVIN.
Source of TVVOUT: fixed to VCRVIN (or Hi-Z).
Source of TVRC: fixed to VCRRC (or Hi-Z).
Source of TVG: fixed to VCRG (or Hi-Z).
Source of TVB: fixed to VCRB (or Hi-Z).
Source of VCRVOUT: fixed to TVVIN (or Hi-Z).
Source of VCRC: fixed to Hi-Z.

MUTE: Audio output control
0: Normal operation
1: ALL Audio outputs to GND (default)

AUTO: Auto startup bit
0: Auto startup disable (Manual startup).
1: Auto startup enable (default).
Note: When the SBIO1 bit = “1”(default = “0”), the change of AUTO bit may cause a “L” pulse on INT pin.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Switch	VMUTE	0	VCR1	VCR0	MONO	1	TV1	TV0
R/W		R/W							
Default		1	0	0	1	0	1	0	1

TV1-0: TVOUTL/R pins source switch
- 00: AMP
- 01: VCRINL/R pins (default)
- 10: MUTE
- 11: Reserved

MONO: Mono select for TVOUTL/R pins
- 0: Stereo. (default)
- 1: Mono. (L+R)/2

VCR1-0: VCROUTL/R pins source switch
- 00: AMP
- 01: TVINL/R pins (default)
- 10: MUTE
- 11: Volume#1 output

VMUTE: Mute switch for volume #1
- 0: Normal operation
- 1: Mute the volume #1 (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Main volume	0	0	L5	L4	L3	L2	L1	L0
R/W		R/W							
Default		0	0	0	1	1	1	1	1

L5-0: Volume #1 control

Those registers control both Lch and Rch of Volume #1.

111111 to
100011: (Reserved)
100010: Volume gain = +6dB
100001: Volume gain = +4dB
100000: Volume gain = +2dB
011111: Volume gain = +0dB (default)
011110: Volume gain = -2dB
...
000011: Volume gain = -56dB
000010: Volume gain = -58dB
000001: Volume gain = -60dB
000000: Volume gain = Mute

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Volume Control	0	VMONO	CAL	0	0	MOD	MDT1	MDT0
R/W		R/W							
Default		0	0	1	0	0	1	1	1

MDT1-0: The time length control of volume transition time
- 00: typ. 5.3 ms
- 01: typ. 10.7 ms
- 10: typ. 21.3 ms
- 11: typ. 42.7 ms (default)

MOD: Soft transition enable for volume #1 control
- 0: Disable
  The volume value changes immediately without soft transition.
- 1: Enable (default)
  The volume value changes with soft transition.
  This function is disabled when STBY bit = "1".

CAL: Offset calibration Enable
- 0: Offset calibration disable.
- 1: Offset calibration enable (default)

VMONO: Mono select for VCROUTL/R pins
- 0: Stereo. (default)
- 1: Mono. (L+R)/2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Video switch	0	0	VVCR2	VVCR1	VVCR0	VTV2	VTV1	VTV0
R/W		R/W							
Default		0	0	0	1	1	1	0	0

VTV2-0: Selector for TV video output
Refer Table 10.

VVCR2-0: Selector for VCR video output
Refer Table 11.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Output Enable	CIO	TVFB	VCRC	VCRV	TVB	TVG	TVR	TVV
R/W		R/W							
Default		0	0	0	0	0	0	0	0

TVV: TVVOUT output control
TVR: TVRCOUT output control
TVG: TVGOUT output control
TVB: TVBOUT output control
VCRV: VCRVOUT output control
VCRC: VCRC output control
TVFB: TVFB output control
0: Hi-Z (default)
1: Active.

CIO: VCR RGB I/O control for VCR SCART
Refer Table 12.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Video volume	CLAMPB	VCLP1	VCLP0	CLAMP2	CLAMP1	CLAMP0	0	0
R/W		R/W							
Default		0	0	0	0	0	1	0	0

CLAMPB, CLAMP2-0: Clamp control.
Refer Table 13, Table 14 and Table 15.

VCLP1-0: DC restore source control
00: ENCV pin (default)
01: ENCY pin
10: VCRVIN pin
11: (Reserved)
When the AUTO bit = "1", the source is fixed to VCRVIN pin.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	S/F Blanking	SBIO1	SBIO0	SBV1	SBV0	SBT1	SBT0	FB1	FB0
R/W		R/W							
Default		0	0	0	0	0	0	0	0

FB1-0: TV Fast Blanking output control (for TVFB pin)
00: 0V (default)
01: 2V<, 2.5V(typ) at 150Ω load
10: follow VCR FB input (2.5V/0V)
11: (Reserved)

SBT1-0: TV Slow Blanking output control (for TVSB pin. minimum load is 10kΩ.)
00: < 2V (default)
01: 4.73V <, < 7V
10: (Reserved)
11: 10V <

SBV1-0: VCR Slow Blanking output control (for VCRSB pin. minimum load is 10kΩ.)
00: < 2V (default)
01: 4.73V <, < 7V
10: (Reserved)
11: 10V <

SBIO1-0: TV/VCR Slow Blanking I/O control
Refer Table 20.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Monitor	0	0	FVCR1	TVMON	VCMON	FVCR0	SVCR1	SVCR0
R/W		READ							
Default		0	0	0	0	0	0	0	0

SVCR1-0, FVCR1-0: VCR fast blanking/slow blanking monitor
Refer Table 21, Table 22.

VCMON, TVMON: VCR/TV video input monitor
Refer Table 23.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Monitor mask	MCOMN	0	0	MTV	MVC	MFVCR	MSVCR	0
R/W		R/W							
Default		0	0	0	0	1	0	0	0

MSVCR: SVCR1-0 bits Monitor mask
0: The INT pin reflects the change of SVCR1-0 bit. (default)
1: The INT pin does not reflect the change of SVCR1-0 bits.

MFVCR: FVCR Monitor mask
0: The INT pin reflects the change of MFVCR bit. (default)
1: The INT pin does not reflect the change of MFVCR bit.

MVC: VCR input monitor mask
Refer Table 25.

MTV: TV input monitor mask
Refer Table 24.

MCOMN: Monitor mask option
Refer Table 23.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	DC restore	0	0	0	0	VCLP2	0	1	1
R/W		R/W							
Default		0	0	0	0	0	0	1	1

VCLP2: DC restore source control
Refer Table 16

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Main volume	0	VOL3	VOL2	VOL1	VOL0	1	1	1
R/W		R/W							
Default		0	0	0	1	1	1	1	1

VOL3-0: Volume #0 control
Those registers control both Lch and Rch of Volume #0.
1011: Volume gain = +24dB
1010: Volume gain = +21dB
1001: Volume gain = +18dB
1000: Volume gain = +15dB
0111: Volume gain = +12dB
0110: Volume gain = +9dB
0101: Volume gain = +6dB
0100: Volume gain = +3dB
0011: Volume gain = +0dB (default)
0010: Volume gain = -3dB
0001: Volume gain = -6dB
0000: MUTE

SYSTEM DESIGN

Figure 20 shows the system connection diagram example. The evaluation board AKD4709 demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

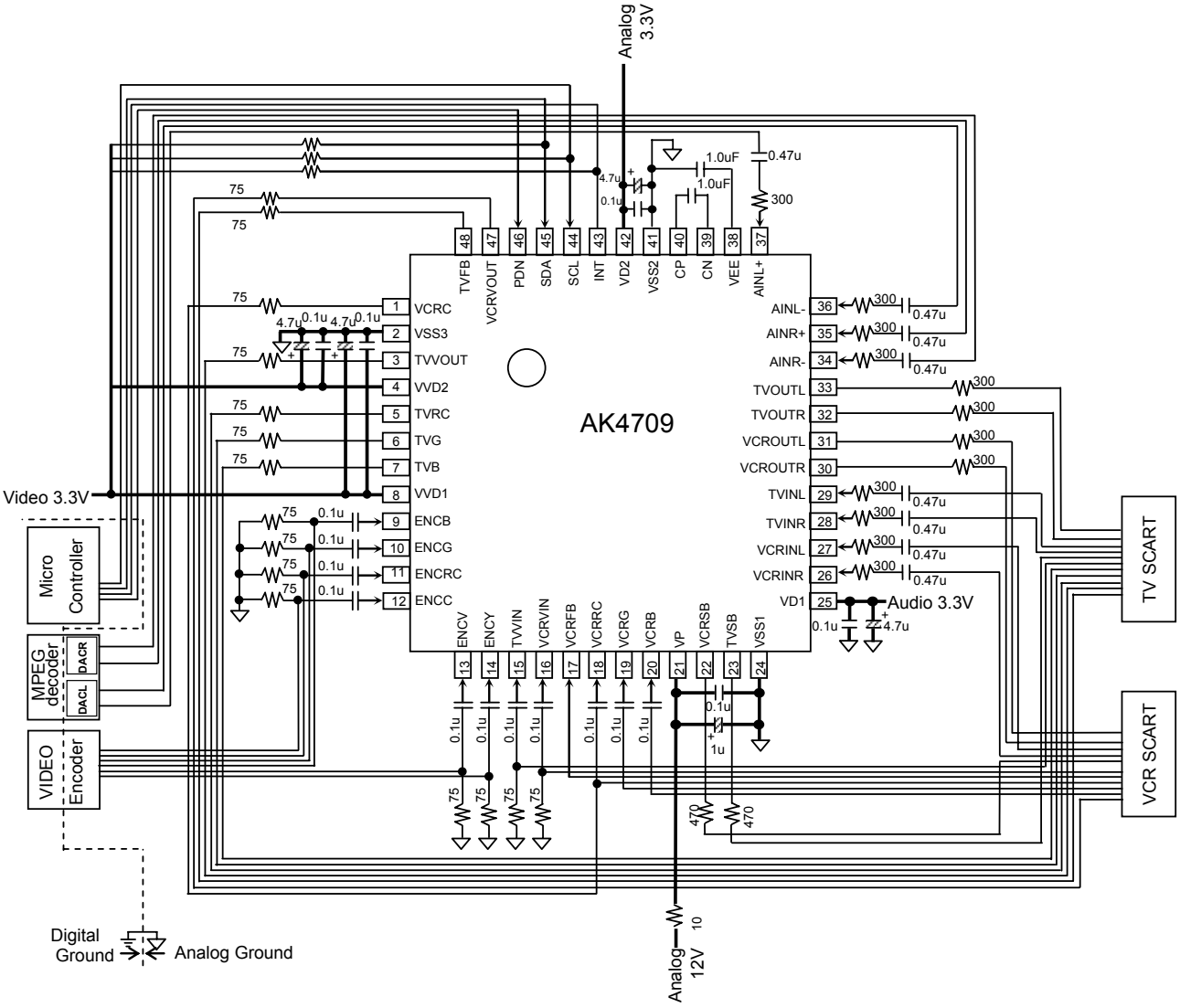


Figure 20. Typical Connection Diagram

■ Grounding and Power Supply Decoupling

VD1, VD2, VP, VVD1, VVD2, VSS1, VSS2 and VSS3 should be supplied from analog supply unit with low impedance and be separated from system digital supply. An electrolytic capacitor 4.7μF parallel with a 0.1μF ceramic capacitor should be attached to VD1, VD2, VVD1, VVD2, VSS1, VSS2 and VSS3 pin to eliminate the effects of high frequency noise. The 0.1μF ceramic capacitor should be placed as near to VD1 (VD2, VVD1, VVD2) as possible.

The VP pin must be connected to the Analogue 12V power supply via a 10ohm resistor and with a 0.1μF ceramic capacitor in parallel with a 1μF electrolytic capacitor to VSS1, as shown in Figure 20.

■ Analog Audio Outputs

The analog outputs are also single-ended and centered on 0V(typ.). The output signal range is typically 2Vrms .

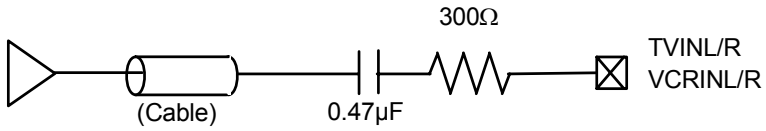
■ Slow Blanking pins

The Slow Blanking Pin must have a 470ohm ±5% series resistor.

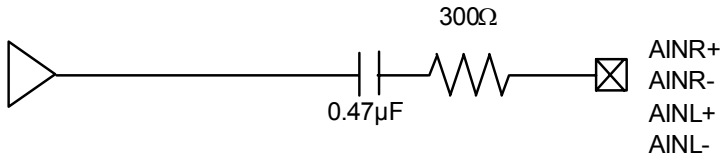
■ External Circuit Example

The analog audio input pin must have 300ohm series resistor and 0.47uF capacitor.

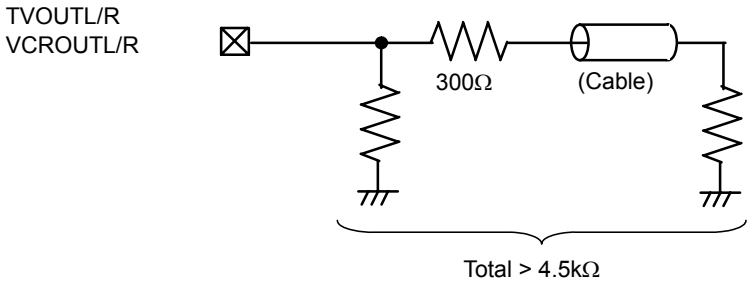
Analog Audio Input pin



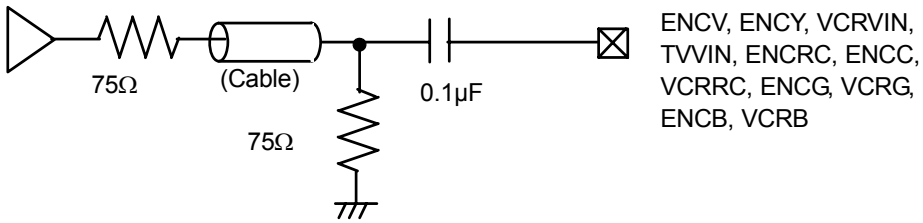
Analog Audio Input pin



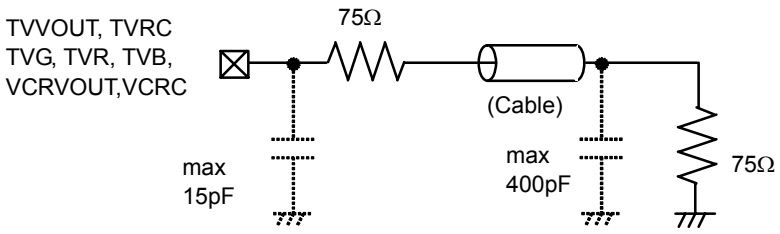
Analog Audio Output pin



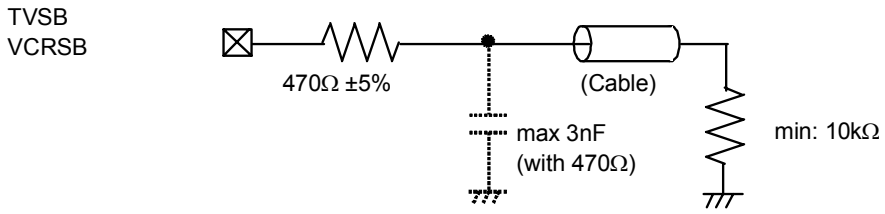
Analog Video Input pin



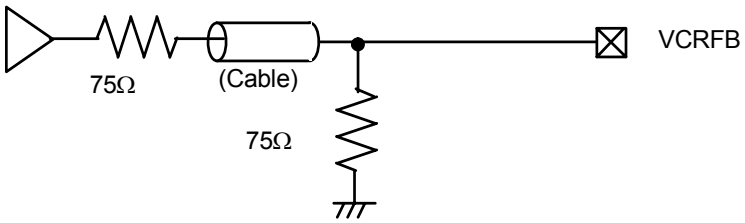
Analog Video Output pin



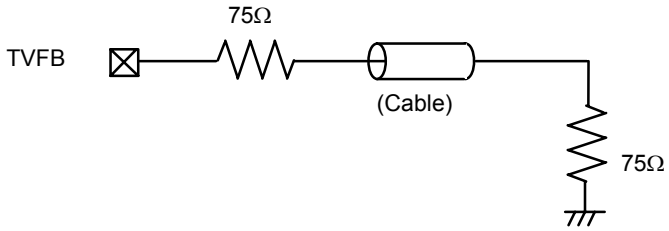
Slow Blanking pin



Fast Blanking Input pin

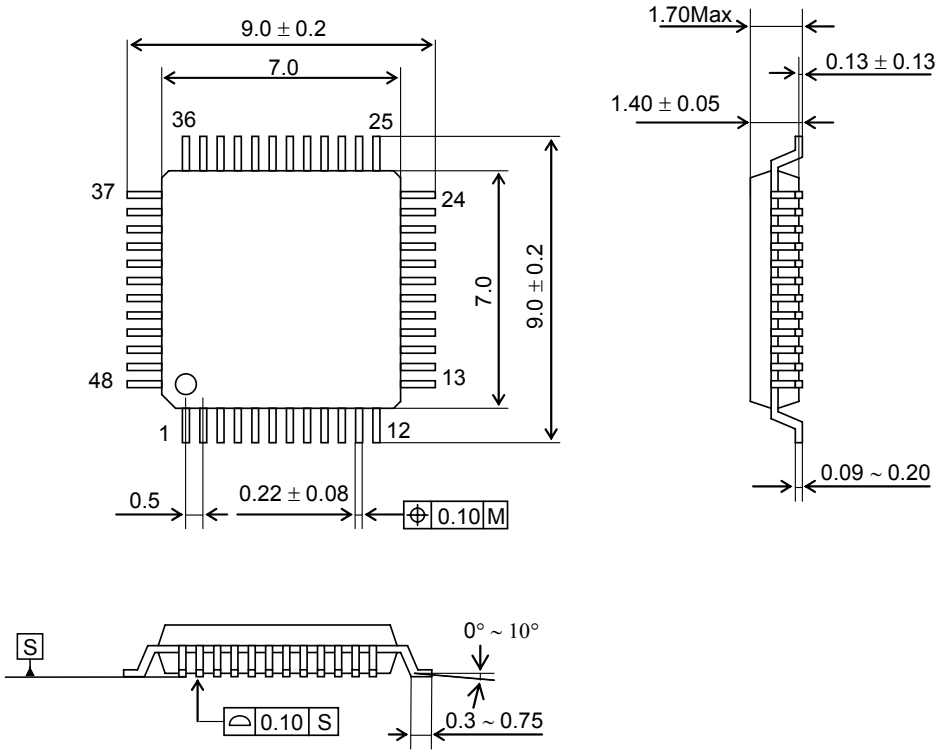


Fast Blanking Output pin



PACKAGE

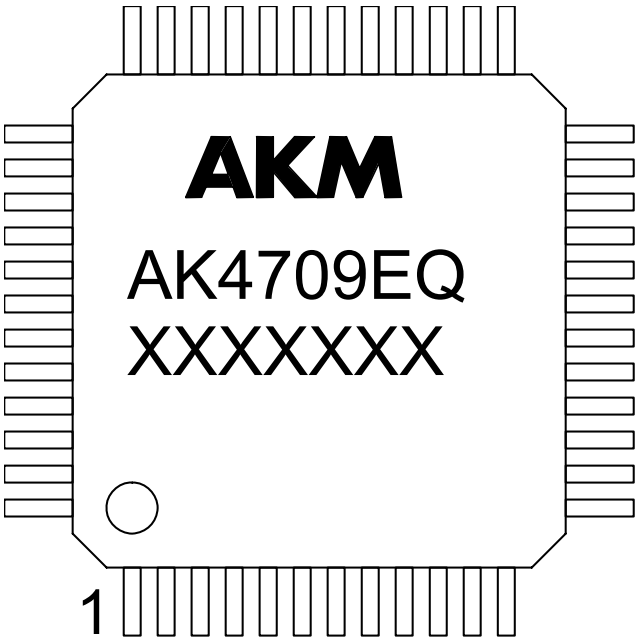
48pin LQFP (Unit: mm)



■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



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REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
11/07/28	00	First Edition		

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